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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): SATO et al

Serial No.: Rule 1.53(b) continuation of U.S. Patent Application Serial No. 09/709,403 filed November 13, 2000

Filed: Herewith

For: METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Group of Parent: 2813

Examiner of Parent: W. Vesperman

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 26, 2003

Sir:

Pursuant to the requirements of 35 USC §119 and 37 CFR §1.55, Applicants hereby claim the right of priority based on Patent Application No. 2000-012026, filed in Japan on January 20, 2000.

A certified copy of the above-identified Japanese patent application was submitted on November 13, 2000, in prior application Serial No. 09/709,403, filed November 13, 2000.

Respectfully submitted,

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日 本 国 特 許 庁
PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日
Date of Application: ２０００年 １月２０日

出 願 番 号
Application Number: 特願２０００－０１２０２６

出 願 人
Applicant (s): 株式会社日立製作所
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２０００年 ９月２２日

特 許 庁 長 官
Commissioner,
Patent Office 及川耕造

出証番号 出証特２０００－３０７６６８０